In the Claims:

Please amend claims 1, 5-9, 18, 23-26, 30, and 41, as specified below. The current status of the claims follows:

1. (currently amended) An integrated circuit (IC) including redundancy circuitry configured to provide redundancy by using a decoder circuitry coupled to a set of storage circuits, wherein the decoder circuitry is configured to decode coded defect information received from a set of circuit elements adapted to provide the coded defect information.

2. (original) The integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy by bypassing a defective circuit block within the integrated circuit (IC).

3. (original) (original) The integrated circuit (IC) according to claim 2, wherein the redundancy circuitry is further configured to provide redundancy by using a redundant circuit block to perform the functionality of the bypassed defective circuit block.

4. (original) The integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy for a plurality of circuit blocks within the integrated circuit (IC).

5. (currently amended) The integrated circuit (IC) according to claim ~~3~~ 4, wherein the set of circuit elements comprise a plurality of programmable circuit elements.

6. (currently amended) The integrated circuit (IC) according to claim ~~3~~ 5, wherein ~~the~~ a number of the plurality of programmable circuit elements is smaller than the number of the circuit blocks in the plurality of circuit blocks.

7. (currently amended) The integrated circuit (IC) according to claim ~~6~~ 5, wherein each of the programmable circuit elements comprises an electrically programmed fuse.

8. (currently amended) The integrated circuit (IC) according to claim ~~6~~ 5, wherein each of the programmable circuit elements comprises a laser-programmed fuse.

9. (currently amended) An integrated circuit (IC), comprising:

means for providing coded signals that correspond to a defect in a defective circuitry within the integrated circuit;

means for decoding the coded signals to generate decoded defect signals and for providing the decoded defect signals to means for storage of signals; and

means for providing redundancy in the integrated circuit in response to the decoded defect signals.

10. (original) The integrated circuit (IC) according to claim 9, wherein the number of decoded defect signals is larger than the number of coded signals.

11. (original) The integrated circuit (IC) according to claim 10, wherein, in response to the decoded defect signals, the means for providing redundancy in the integrated circuit causes a redundant circuitry to be used instead of the defective circuitry.

12. (original) The integrated circuit (IC) according to claim 11, wherein the means for providing the coded signals couples to the means for decoding the coded signals via a first signal link.

13. (original) The integrated circuit (IC) according to claim 12, wherein the means for decoding the coded signals couples to the means for providing redundancy via a second signal link.

14. (original) The integrated circuit (IC) according to claim 13, wherein the defective circuitry comprises a memory circuit.

15. (original) The integrated circuit (IC) according to claim 14, wherein the redundant circuitry comprises a memory circuit.

16. (original) The integrated circuit (IC) according to claim 15, wherein the means for providing redundancy couples to the defective circuitry via a third signal link.

17. (original) The integrated circuit (IC) according to claim 16, wherein the means for providing redundancy couples to the redundant circuitry via a fourth signal link.

18. (currently amended) A programmable logic device (PLD), comprising:

a plurality of programmable elements, the plurality of programmable elements configured to provide a first set of signals;

a decoder circuit coupled to the plurality of programmable elements, the decoder circuit configured to derive a second set of signals from the first set of signals and to provide the second set of signals to a shift register; and

redundancy circuitry coupled to the decoder circuit,

wherein the redundancy circuitry is responsive to the second set of signals.

19. (original) The programmable logic device (PLD) according to claim 18, wherein the first set of signals comprises a set of signals configured to identify a defective circuit in the programmable logic device (PLD).

20. (original) The programmable logic device (PLD) according to claim 19, wherein the set of signals configured to identify the defective circuit comprises coded signals.

21. (original) The programmable logic device (PLD) according to claim 20, further comprising a redundant circuit, wherein, in response to the second set of signals, the redundancy circuitry causes an input signal to be coupled to the redundant circuit instead of the defective circuit.

22. (original) The programmable logic device (PLD) according to claim 21, wherein, in response to the second set of signals, the redundancy circuitry causes an output signal of the redundant circuit to be used instead of an output signal of the defective circuit.

23. (currently amended) The programmable logic device (PLD) according to claim 22, wherein the ~~coding of the~~ coded signals ~~corresponds~~ correspond to information programmed in the programmable elements.

24. (currently amended) The programmable logic device (PLD) according to claim ~~23~~ 18, wherein each of the programmable elements comprises a fuse.

25. (currently amended) The programmable logic device (PLD) according to claim ~~24~~ 18, wherein each fuse comprises an electrically programmed fuse.

26. (currently amended) The programmable logic device (PLD) according to claim ~~24~~ 18, wherein each fuse comprises a laser-programmed fuse.

27. (original) The programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises a memory circuit, and wherein the redundant circuit comprises a memory circuit.

28. (original) The programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises programmable logic circuitry, and wherein the redundant circuit comprises programmable logic circuitry.

29. (original) The programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises programmable interconnect circuitry, and wherein the redundant circuit comprises programmable interconnect circuitry.

30. (currently amended) A programmable logic device (PLD), comprising:

a first block of memory;

a plurality of programmable fuses, the plurality of programmable fuses configured to provide a set of coded signals corresponding to a defect in the first block of memory;

a decoder circuit configured to derive a decoded set of signals from the coded set of signals;

a plurality of flip-flops coupled to the decoder circuit, the plurality of flip-flops configured to receive the decoded set of signals;

redundancy circuitry coupled to the decoder circuit, the redundancy circuitry configured to respond to the decoded set of signals; and

a second block of memory coupled to the redundancy circuitry,

wherein the second block of memory is used to provide redundancy for the first block of memory.

31. (original) The programmable logic device (PLD) according to claim 30, wherein each fuse in the plurality of fuses comprises an electrically programmed fuse.

32. (original) The programmable logic device (PLD) according to claim 30, wherein each fuse in the plurality of fuses comprises a laser-programmed fuse.

33. (original) The programmable logic device (PLD) according to claim 30, wherein the decoder comprises:

at least one inverter adapted to receive the coded signals; and

at least one AND gate coupled to the at least one inverter,

wherein the at least one AND gate provides the decoded set of signals.

34. (original) The programmable logic device (PLD) according to claim 30, wherein the redundancy circuitry comprises a set of flip-flops configured to receive the decoded set of signals from the decoder circuit.

35. (original) The programmable logic device (PLD) according to claim 34, wherein the redundancy circuitry further comprises a set of OR gates, wherein each OR gate in the set of OR gates couples to a respective flip-flop in the set of flip-flops.

36. (original) The programmable logic device (PLD) according to claim 35, wherein the redundancy circuitry further comprises a set of multiplexers, wherein each multiplexer in the set of multiplexers couples to a respective OR gate in the set of OR gates.

37. (original) The programmable logic device (PLD) according to claim 36, wherein a first multiplexer in the set of multiplexers couples to the first block of memory.

38. (original) The programmable logic device (PLD) according to claim 37, wherein a second multiplexer in the set of multiplexers couples to the second block of memory.

39. (original) The programmable logic device (PLD) according to claim 30, further comprising programmable logic circuitry coupled to the second memory block.

40. (original) The programmable logic device (PLD) according to claim 30, further comprising programmable interconnect circuitry coupled to the second memory block.

41. (currently amended) A method of providing redundancy in an integrated circuit (IC), the method comprising:

retrieving information about a defect in the integrated circuit (IC), wherein the information about the defect is coded in the integrated circuit (IC);

decoding the information about the defect to identify a defective circuit within the integrated circuit (IC);

receiving a scan chain testing signal; and

using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit.

42. (original) The method according to claim 41, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information coded in a set of programmable elements within the integrated circuit (IC).

43. (original) The method according to claim 42, wherein decoding the information about the defect to identify a defective circuit within the integrated circuit (IC) further comprises generating a set of decoded signals from the information about the defect.

44. (original) The method according to claim 43, wherein the number of signals in the set of decoded signals is larger than the number of programmable elements in the set of programmable elements.

45. (original) The method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises bypassing the identified defective circuit.

46. (original) The method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises routing a set of input/output signals to the redundant circuit instead of the identified defective circuit.

47. (original) The method according to claim 46, wherein routing a set of input/output signals to the redundant circuit instead of the identified defective circuit further comprises:

routing an input signal to the redundant circuit instead of the identified defective circuit; and

using an output signal of the redundant circuit instead of an output signal of the identified defective circuit.

48. (original) The method according to claim 43, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information that is generated by testing the integrated circuit (IC) to identify a defective circuit, and coding the information about the defect in the set of programmable elements.

49. (original) The method according to claim 48, wherein the integrated circuit (IC) comprises a programmable logic device (PLD).

50. (original) The method according to claim 49, wherein the defective circuit comprises a memory circuit within the programmable logic device (PLD).

51. (original) The method according to claim 50, wherein the defective circuit comprises programmable logic circuitry within the programmable logic device (PLD).

52. (original) The method according to claim 50, wherein the defective circuit comprises programmable interconnect circuitry within the programmable logic device (PLD).